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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,393	09/25/2003	David Muller	1406/168	9168

25297 7590 09/16/2004

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EXAMINER	
LE, DON P	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 09/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,393	MULLER ET AL.	
	Examiner	Art Unit	
	Don P Le	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/2/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 10-15* is/are rejected.

7)☒ Claim(s) *3-9, 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2 and 10-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Baker (US 5,953,276).

3. With respect to claims 1 and 11, figure 3 of Baker discloses an apparatus for converting a differential logic input signal and a corresponding common mode differential logic signal each having a first single-ended logic signal and a complementary second single-ended logic signal to a single-ended logic output signal comprising:

(a) a first differential stage having a first PMOS transistor (Q1) and a second PMOS transistor (Q5) wherein the gate terminal of the first PMOS transistor is coupled to the first single-ended signal (+VIN) of the common mode level differential signal, wherein the gate terminal of the second PMOS transistor is coupled to the second single-ended signal (-VIN) of the common mode level differential signal, and wherein the source terminals of the PMOS transistors are connected to a first current source (Q4);

(b) a second differential stage having a first NMOS transistor (Q2) and a second NMOS transistor (Q6) wherein the gate terminal of the first NMOS

transistor is coupled to the first single-ended signal of the differential input signal, wherein the gate terminal of the second NMOS transistor is coupled to the second single-ended signal of the differential input signal, and wherein the source terminals of the NMOS transistors are connected to a second current source (Q3), and wherein the drain terminals of the NMOS transistors are connected to the drain terminals of the PMOS transistors;

(c) an output (+VOUT) connected to the source terminal of the second PMOS transistor and to the drain terminal of the second NMOS transistor for providing the single-ended output signal;

(d) wherein the current sources are controlled by a voltage level that is centered between the mid-potentials of the common mode level differential logic signal and the mid-potential of the differential logic input signal such that both current sources deliver the same constant current (circuit providing current controlled, 18).

4. With respect to claim 2, figure 3 of Baker teaches the apparatus further comprises a complementary output between the drain terminal of the first PMOS transistor and the connected drain terminal of the first NMOS transistor for providing an inverted single-ended output signal.

5. With respect to claim 10, figure 3 of Baker discloses an inverter (24) connected to the outputs.

6. With respect to claims 12-15, the apparatus of Baker is a differential amplifier design with CMOS integrated circuit. Therefore, the claimed properties are inherent in the apparatus of Baker. It is well known in the art that size-ratio of transistors are chosen for particular design.

Allowable Subject Matter

7. Claims 3-9 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is an examiner's statement of reasons for allowance:

With respect to claim 3, the prior art does not teach resistors connected in series between gate terminal of the first PMOS and the second PMOS transistors.

With respect to claim 7, the prior art does not teach pair of NMOS transistors connected in series between gate terminal of the first PMOS and the second PMOS transistors.

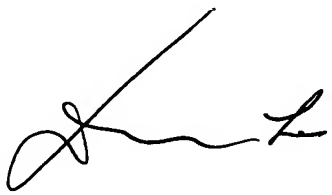
Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P Le whose telephone number is 571-272-1806. The examiner can normally be reached on 7AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

9/10/2004



DON LE
PRIMARY EXAMINER